IN THE CLAIMS:

1. (amended) A system for testing a collection of device chips by temporarily attaching a microjoint structure to the array comprising:

the microjoint function carrier having a multilayer substrate ~~having~~ with a plurality of receptacles in its top surface;

a set of ~~microdentritic~~ dendritic features disposed ~~on~~ in said receptacles;

a set of contact pads on the device chips that match the plurality of receptacles ~~on~~ in the carrier;

a set of test pads on the carrier, and

interconnect wiring that connects the test pads to the ~~microdentritic~~ dendritic pad array.

2. (amended) A system as defined in Claim 1, wherein the contact pads on the device chips are shaped to have studs extending from the respective pad surfaces.

3. (original) A system as defined in Claim 1, wherein the receptacles have contiguous layers of liner, seed and barrier at their interior walls and bases, in addition to noble metal dendrites at the innermost portions of these surfaces.

4. (amended) A system as in Claim 3 wherein the liner layer is selected from the group consisting of Ta, Ti, W, TaN, TiN, WN, Cr~~,~~, with a thickness of 200-1600A.

5. (amended) A system as in Claim 3 wherein the seed layer is selected from the group consisting of Cu, Au~~,~~, with a thickness of 300-2000A.

6. (amended) A system as in Claim 3 wherein the barrier layer is selected from the group consisting of Ni, Ni-P, Co, Co-P, Ni-P, Pt, Pd~~,~~, with a thickness of 2000-10,000A.

7. (original) A system as defined in Claim 1, wherein the carrier includes a layer of silicon and a dielectric layer, the receptacles being in the dielectric layer, and carrier wiring being beneath the dielectric layer.

8. (original) A system as defined in Claim 4, wherein the liner layer is etched away from the top surface of the dielectric layer.

9. (original) A system as defined in Claim 5, wherein the seed layer is etched away from the top surface of the dielectric layer.

10. (original) A system as in Claim 1 wherein said dendrites are made of a noble metal selected from the group comprising Pt, Pd, Rh.

11. (original) A system as in Claim 6 wherein the metal of dendrites is selected from non-noble metals such as Ni, Cu, and subsequently plated over with a noble metal such as Pt, Pd, Rh.

12. (amended) A process for testing an array of device chips in a semiconductor wafer by temporarily attaching a microjoint structure to the array comprising:

forming the microjoint structure by building a carrier in the form of a multilayer substrate and having a plurality of receptacles on the carrier;

forming a set of contact pads on the device chips;

forming a set of ~~microdentritic~~ dendritic pad arrays on a carrier, matching the contact pads on the device chips;

forming interconnect wiring on the carrier that connects the contact pads to the ~~microdentritic~~ dendritic pad array;

assembling the chips to temporarily engage contact pads on the chip against matching ~~microdendritic~~ dendritic pads on the carrier to make temporary contact, and

performing system level functional tests and burn-in on the entire collection of chips.

13. (amended) A process as defined in Claim 12 including ~~the~~ a step of forming contact pads at the ends of studs extending from the semiconductor wafer.

14. (amended) A process as defined in Claim 12 including ~~the~~ a step of forming contiguous layers of liner, seed, barrier metal and noble metal dendritic layers at the peripheries of the receptacle in the top surface of the carrier.

15. (amended) A process as defined in Claim 14 wherein the liner layer is selected from the group consisting of Ta, Ti, W, TaN, TiN, WN,Cr~~,~~ with a thickness of 200-1600A.

16. (amended) A process as defined in Claim 14 wherein the seed layer is selected from the group consisting of Cu, Au~~,~~ with a thickness of 300-2000A.

17. (amended) A process as defined in Claim 14 wherein the barrier layer is selected from the group consisting of Ni, Ni-P, Co, Co-P, Ni-P, Pt, Pd~~,~~ with a thickness of 2000-1000A.

18. (original) A process as defined in Claim 14, wherein the carrier includes a layer of silicon and a dielectric layer, the receptacles being in the dielectric layer, and carrier wiring is below the dielectric layer.

19. (original) A process as defined in Claim 18, including the step of etching away the liner layer from the top surface of the tantalum layer.

20. (original) A process in accordance with Claim 18, including the step of etching away the seed away from the top surface of the dielectric layer.

21. (original) A process as defined in Claim 14 wherein the noble metal constituting the dendrites is selected from the group comprising Pt, Pd, Rh.

22. (original) A process as defined in Claim 14 wherein the metal constituting the dendrites is selected from the group comprising Ni, Cu, and subsequently plated over by a layer of noble metal such as Pt, Pd, Rh.